module ram\_tb;

reg clk;

reg write\_enable;

reg [9:0]address;

reg [7:0]data\_in;

wire [7:0]data\_out;

ram uut(clk,write\_enable,address,data\_in,data\_out);

initial begin

clk = 0;

data\_in = 8'h56;

write\_enable = 0;

address = 55;

#20

write\_enable = 1;

#20;

write\_enable = 0;

address = 66;

data\_in = 8'h36;

#20

write\_enable = 1;

#20

write\_enable = 0;

#20

address = 55;

#20

$finish();

end

**always** #10 clk = ~clk; //clock generation

endmodule